RING OSCILLATOR WITH PEAKING STAGES

BACKGROUND OF THE INVENTION
TECHNICAL FIELD OF THE INVENTION

[0001]   This invention relates generally to communication systems and more particularly to oscillator circuits used therein.

DESCRIPTION OF RELATED ART

[0002]   Communication systems are known to transport large amounts of data between a plurality of end user devices, which, for example, include telephones, facsimile machines, computers, television sets, cellular telephones, personal digital assistants, etc. As is known, such communication systems may be local area networks (LANs) and/or wide area networks (WANs) that are stand-alone communication systems or interconnected to other LANs and/or WANs as part of a public switched telephone network (PSTN), packet switched data network (PSDN), integrated service digital network (ISDN), or Internet. As is further known, communication systems include a plurality of system equipment to facilitate the transporting of data. Such system equipment includes, but is not limited to, routers, switches, bridges, gateways, protocol converters, frame relays, and private branch exchanges.

[0003]   The transportation of data within communication systems is governed by one or more standards that ensure the integrity of data conveyances and fairness of access for data conveyances. For example, there are a variety of Ethernet standards that govern serial transmissions within a communication system at data rates of 10 megabits-per-second, 100 megabits per second, 1 gigabit per second and beyond. Synchronous Optical NETwork (SONET), for example, currently provides for up to 10 gigabits per second. In accordance with such standards, many system components and end user devices of a communication system transport data via serial

transmission paths. Internally, however, the system
components and end user devices may process data in a
parallel manner. As such, each system component and end user
device must receive the serial data and convert the serial
data into parallel data without loss of information. After
processing the data, the parallel data must be converted back
to serial data for transmission without loss.

[0004]   Accurate recovery of information from high-speed
serial transmissions typically requires transceiver
components that operate at clock speeds equal to or higher
than the received serial data rate. Higher clock speeds
require oscillator circuits to have gain-bandwidth products
to sustain high frequency oscillations while maintaining low
phase noise. High phase noise contributes to clock jitter
which degrades clock recovery in high speed circuits. Higher
clock speeds limit the usefulness of prior art clock recovery
circuits that require precise alignment of signals to recover
clock and/or data. Higher data rates require greater
bandwidth for a feedback loop of the clock recovery circuits
to operate correctly. Some prior art designs are bandwidth
limited.

[0005]   As the demand for data throughput increases, so do
the demands on a high-speed serial transceiver. The
increased throughput demands are pushing some current
integrated circuit manufacturing processes to their operating
limits. Integrated circuit processing limits (e.g., device
parasitics, trace sizes, propagation delays, device sizes)
and integrated circuit (IC) fabrication limits (e.g., IC
layout, frequency response of the packaging, frequency
response of bonding wires) limit the speed at which the high-
speed serial transceiver may operate without excessive jitter
performance and/or noise performance.

[0006]   A further alternative for high-speed serial
transceivers is to use an IC technology that inherently
provides for greater speeds. For instance, switching from a
CMOS process to a silicon germanium or gallium arsenide

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process would allow integrated circuit transceivers to operate at greater speeds, but at substantially increased manufacturing costs. CMOS is more cost effective and provides easier system integration. Currently, for most commercial-grade applications, including communication systems, such alternate integrated circuit fabrication processes are too cost prohibitive for widespread use.

[0007] Modern communication systems, typically include a plurality of circuit boards that communicate with each other by way of signal traces, bundled data lines, back planes, etc. Accordingly, designers of high data rate communication transceiver devices often have conflicting design goals that relate to the performance of the particular device. For example, there are many different communication protocols specified for data rates that range from 2.48832 gigabits per second for OC48, to 9.95 gigabits per second for OC192. Other known standards define data rates of 2.5 gigabits per second (INFINIBAND) or 3.125 gigabits per second (XAUI). For example, one protocol may specify a peak voltage range of 200-400 millivolts, while another standard specifies a 500-700 millivolts mutually exclusive voltage range of 500-700 millivolts mutually exclusive requirements (and therefore cannot support multiple protocols) or must design a high data rate transceiver device that can adapt according to the protocol being used for the communications.

[0008] Along these lines, field programmable gate array (FPGA) circuits are gaining in popularity for providing the required flexibility and adaptable performance described above for those designers that seek to build one device that can operate according to multiple protocols. Thus, while FPGA technology affords a designer an opportunity to develop flexible and configurable hardware circuits, specific designs that achieve the desired operations must still be developed. Accordingly, there is a need for oscillator circuits within a

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transceiver device that achieves these design objectives. While traditional phase-locked loops include mechanical oscillators that produce an oscillation based on a current, integrated circuit designs desirably include oscillators formed from integrated circuit devices. There is a need therefore, for an integrated circuit based oscillator that provides the desired oscillations in a variable manner within specified noise constraints.

BRIEF SUMMARY OF THE INVENTION

[0009]   An embodiment of the present invention includes a delay stage circuit of a ring oscillator for setting a delay value of the delay stage circuit and a corresponding frequency of operation of the ring oscillator. The delay stage circuit comprises a differential transistor pair for receiving an input oscillation signal and for producing a corresponding output oscillation signal characterized by a delay. The differential transistor pair is coupled to receive a bias signal, set by an external bias circuit, to provide a fine delay adjustment to a selectable frequency of oscillation set by an active load.

[0010]   In one embodiment, the active load, comprising a pair of MOSFET devices coupled to a selectable resistive load, generates an R-C time constant of the active load that defines the delay of the differential transistor pair. A fixed capacitance is provided by the structure of the pair of MOSFET devices. Because the resistive load has selectable resistance values, the R-C time constant of the active load is adjustable. As the R-C time constant affects an amount of delay of the output oscillation signal relative to the input oscillation signal, a frequency of oscillation may be set by the resistive devices coupled within the active load.

[0011]   In one embodiment, a plurality of resistive and capacitive devices are selectively coupled to the active load to define the delay of the differential transistor pair. The frequency of oscillation of the ring oscillator is a function

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of the delay of each delay stage circuit of the ring
oscillator as set by the selectable active loads and a
function of the externally provided bias signal. The bias
signal adjusts a bias level of the differential transistor
pair by opening or closing at least one of a plurality of
selectable switches thereby adjusting a response time and
associated delay through the transistor pair. The logic to
close one of the plurality of selectable switches operates
under one of manual control or automatic control to select
the ring oscillator frequency of oscillation.

[0012]   In each embodiment of the invention, responsive to
resistive and capacitive devices values, whether permanently
or selectively coupled, the differential transistor pair will
produce an output oscillation signal that has a peak response
at an oscillation frequency that corresponds to the R-C time
constant set by the resistive and capacitive values.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013]   Figure 1 is a schematic block diagram of a
programmable logic device that includes programmable logic
fabric and a plurality of programmable multi-gigabit
transceivers (PMGTs) and a control module;

[0014]   Figure 2 is a schematic block diagram of one
embodiment of a representative one of the programmable multi-
gigabit transceivers;

[0015]   Figure 3 illustrates an alternate schematic block
diagram of a representative one of the programmable multi-
gigabit transceivers;

[0016]   Figure 4A illustrates a schematic block diagram of
the programmable receive PMA module that includes a
programmable front-end, a data and clock recovery module, and
a serial-to-parallel module;

[0017]   Figure 4B illustrates a schematic block diagram of
a programmable transmit PMA module that includes a phase
locked loop, a parallel-to-serial module, and line driver;

[0018]   Figure 5 is a schematic block diagram of a ring oscillator according to an embodiment of the present invention;

[0019]   Figure 6 is a schematic block diagram of an NMOS delay stage circuit according to one embodiment of the present invention;

[0020]   Figure 7 is a schematic block diagram of the delay stage of Figure 6 illustrating the adjustment of selectable resistive load R_L to set an oscillation frequency;

[0021]   Figure 8 is a schematic block diagram illustrating gate-to-source capacitance in an N-channel MOSFET;

[0022]   Figure 9 is a graph of an NMOS delay stage frequency response according to one embodiment of the present invention;

[0023]   Figure 10 is a schematic block diagram of an alternate embodiment of the present invention;

[0024]   Figure 11 is a schematic block diagram of a PMOS delay stage circuit according to an alternate embodiment of the present invention;

[0025]   Figure 12 is a graph of a PMOS delay stage response according to one embodiment of the present invention; and

[0026]   Figure 13 is a flow chart of a method according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0027]   Figure 1 is a schematic block diagram of a programmable logic device 10 that includes programmable logic fabric 12, a plurality of programmable multi-gigabit transceivers (PMGTs) 14-28 and a control module 30. The programmable logic device 10 may be a programmable logic array device, a programmable array logic device, an erasable programmable logic device, and/or a field programmable gate array (FPGA). When the programmable logic device 10 comprises an FPGA, the programmable logic fabric 12 may be implemented as a symmetric array configuration, a row-based configuration, a sea-of-gates configuration, and/or a

hierarchical programmable logic device configuration. The
programmable logic fabric 12 may further include at least one
dedicated fixed processor, such as a microprocessor core, to
further facilitate the programmable flexibility offered by
programmable logic device 10.

[0028]   The control module 30 may be contained within the
programmable logic fabric 12 or it may be a separate module.
In either implementation, control module 30 generates control
signals to program transmit and receive sections of each of
the PMGTs 14-28. In general, each of the PMGTs 14-28
performs a serial-to-parallel conversion on receive data and
performs a parallel-to-serial conversion on transmit data.
The parallel data may be, for instance, 8-bits wide, 16-bits
wide, 32-bits wide, or 64-bits wide.

[0029]   Typically, the serial data will be a 1-bit stream
of data that may be a binary level signal, multi-level
signal, etc. Further, two or more programmable multi-gigabit
transceivers may be bonded together to provide greater
transmitting speeds. For example, if PMGTs 14, 16 and 18 are
transceiving data at 3.125 gigabits-per-second, the PMGTs 14,
16 and 18 may be bonded together such that the effective
serial rate is approximately 3 times 3.125 gigabits-per-
second.

[0030]   Each of the programmable multi-gigabit transceivers
14-28 may be individually programmed to conform to separate
standards. In addition, the transmit path and receive path
of each programmable multi-gigabit transceiver 14-28 may be
separately programmed such that the transmit path of a
transceiver is supporting one standard while the receive path
of the same transceiver is supporting a different standard.
Further, the serial rates of the transmit path and receive
path may be programmed, for example, from 1 gigabit-per-
second to tens of gigabits-per-second. The size of the
parallel data in the transmit and receive sections, or paths,
is also programmable and may vary, for instance, from 8-bits,
16-bits, 32-bits, or 64-bits.

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[0031] Figure 2 is a schematic block diagram of one embodiment of a representative one of the programmable multi-gigabit transceivers 14-28. As shown, the programmable multi-gigabit transceiver includes a programmable physical media attachment (PMA) module 32, a programmable physical coding sub-layer (PCS) module 34, a programmable interface 36, a control module 35, a PMA memory mapping register 45 and a PCS register 55. The control module 35, based on the desired mode of operation for the individual programmable multi-gigabit transceiver 14-28, generates a programmed deserialization setting 66, a programmed serialization setting 64, a receive PMA_PCS interface setting 62, a transmit PMA_PCS interface setting 60, and a logic interface setting 58. The control module 35 may be a separate device within each of the programmable multi-gigabit transceivers or included partially or entirely within the control module 30 of Figure 1.

[0032] In either embodiment of the control module 35, the programmable logic device control module 30 determines the corresponding overall desired operating conditions for the programmable logic device 10 and provides the corresponding operating parameters for a given programmable multi-gigabit transceiver to its control module 35, which generates the settings 58-66.

[0033] The programmable physical media attachment (PMA) module 32 includes a programmable transmit PMA module 38 and a programmable receive PMA module 40. The programmable transmit PMA module 38, which will be described in greater detail with reference to Figure 4B, is operably coupled to convert transmit parallel data 48 into transmit serial data 50 in accordance with the programmed serialization setting 64. The programmed serialization setting 64 indicates the desired rate of the transmit serial data 50, the desired rate of the transmit parallel data 48, and the data width of the transmit parallel data 48. The programmable receive PMA module 40 is operably coupled to convert receive serial data

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52 into receive parallel data 54 based on the programmed deserialization setting 66. The programmed deserialization setting 66 indicates the rate of the receive serial data 52, the desired rate of the receive parallel data 54, and the data width of the receive parallel data 54. The PMA memory mapping register 45 may store the programmed serialization setting 64 and the programmed deserialization setting 66.

[0034]   The programmable physical coding sub-layer (PCS) module 34 includes a programmable transmit PCS module 42 and a programmable receive PCS module 44. The programmable transmit PCS module 42 receives transmit data words 46 from the programmable logic fabric 12 via the programmable transmit parallel interface 36 and converts them into the transmit PMA_PCS interface data 48 in accordance with the transmit PMA_PCS interface setting 60. The transmit PMA_PCS interface setting 60 indicates the rate of the transmit data words 46, the size of the transmit data words (e.g., 1-byte, 2-bytes, 3-bytes, 4-bytes) and the corresponding transmission rate of the transmit parallel data 48. The programmable receive PCS module 44 converts the receive parallel data 54 into receive data words 56 in accordance with the receive PMA_PCS interface setting 62. The receive PMA_PCS interface setting 62 indicates the rate at which the receive parallel data 54 will be received, the width of the receive parallel data 54, the transmit rate of the receive data words 56 and the word size of the receive data words 56.

[0035]   The control module 35 also generates the logic interface setting 58 that provides the rates at which the transmit data words 46 and receive data words 56 will be transceived with the programmable logic fabric 12. Note that the transmit data words 46 may be received from the programmable logic fabric 12 at a different rate than the receive data words 56 are provided to the programmable logic fabric 12.

[0036]   As one of average skill in the art will appreciate, each of the modules within the programmable PMA module 32 and

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PCS module 34 may be individually programmed to support a
desired data transfer rate. The data transfer rate may be in
accordance with a particular standard such that the receive
path, i.e., the path through programmable receive PMA module
40 and the programmable receive PCS module 44 may, be
programmed in accordance with one standard, while the
transmit path, i.e., the path through the programmable
transmit PCS module 42 and the programmable transmit PMA
module 38, may be programmed in accordance with the same or
another standard.

[0037]   Figure 3 illustrates an alternate schematic block
diagram of a representative one of the PMGTs 14-28. In this
embodiment, the PMGTs 14-28 include a transmit section 70, a
receive section 72, the control module 35 and the
programmable interface 36. The transmit section 70 includes
the programmable transmit PMA module 38 and the programmable
transmit PCS module 42. The receive section 72 includes the
programmable receive PMA module 40 and the programmable
receive PCS module 44.

[0038]   In this embodiment, the control module 35
separately programs the transmit section and the receive
section via transmit setting 74 and receive setting 76,
respectively. The control module 35 also programs the
programmable interface 36 via the logic interface setting 58.
Accordingly, the control·module 35 may program the receive
section 72 to function in accordance with one standard while
programming the transmit section 70 in accordance with the
same or another standard. Further, the logic interface
setting 58 may indicate that the transmit data words 46 are
received from the programmable logic fabric 12 at a different
rate than the receive data words 56 are provided to the
programmable logic fabric 12. As one of average skill in the
art will appreciate, the programmable interface 36 may
include a transmit buffer and a receive buffer, and/or an
elastic store buffer to facilitate the providing and

receiving of transmit data words 46 and receive data words 56 to and from the programmable logic fabric 12.

[0039]   Figure 4A illustrates a schematic block diagram of the programmable receive PMA module 40 that includes a programmable front-end 100, a data and clock recovery module 102, and a serial-to-parallel module 104. The programmable front-end 100 includes a receive termination circuit 106 and a receive amplifier 108. The data and clock recovery module 102 includes a data detection circuit 110 and a phase locked loop 112. The phase locked loop 112 includes a phase detection module 114, a loop filter 116, a voltage controlled oscillator (VCO) 118, a 1st divider module 120, and a 2nd divider module 122.

[0040]   The programmable front-end 100 is operably coupled to receive the receive serial data 52 and produce amplified and equalized receive serial data 124 therefrom. To achieve this, the receive termination circuit 106 is programmed in accordance with a receive termination setting 126 to provide the appropriate termination for the transmission line between the programmable receive PMA module 40 and the source that originally transmitted the receive serial data 52. The receive termination setting 126 may indicate whether the receive serial data 52 is a single-ended signal, a differential signal, may indicate the impedance of the transmission line, and may indicate the biasing of the receive termination circuit 106. For a more detailed discussion of the receive termination circuit 106, refer to co-pending patent application by Charles W. Boecker et al. entitled RECEIVER TERMINATION NETWORK AND APPLICATION THEREOF, having a filing date the same as the present patent application. This co-pending application is incorporated by reference, herein.

[0041]   The receive termination circuit 106 further biases the receive serial data 52 and provides the bias adjusted signal to the receive amplifier 108. The equalization and gain settings of the receive amplifier 108 may be adjusted in

accordance with equalization setting 128 and amplification setting 130, respectively. Further description of the receiver amplifier 108 may be found in co-pending patent application by William C. Black et al. entitled ANALOG FRONT-END HAVING BUILT-IN EQUALIZATION AND APPLICATIONS THEREOF, having a filing date the same as the present patent application. This co-pending application is incorporated by reference, herein. Note that the receive termination setting 126, the equalization setting 128, and the amplification setting 130 are part of the programmed deserialization setting 66 provided by the control module 35.

[0042]   The data and clock recovery module 102 and the phase detection module 114 of phase-locked loop 112 receive the amplified and equalized receive serial data 124. The phase detection module 114 has been initialized prior to receiving the amplified and equalized receive serial data 124 by comparing the phase and/or frequency of a reference clock 86 with a feedback reference clock produced by divider module 120. Based on this phase and/or frequency difference, the phase detection module 114 produces a corresponding current that is provided to loop filter 116. The loop filter 116 converts the current into a control voltage that adjusts the output frequency of the VCO 118. The divider module 120, based on a serial receive clock setting 132, divides the output oscillation produced by the VCO 118 to produce the feedback signal. Once the amplified and equalized receive serial data 124 is received, the phase detection module 114 compares the phase of the amplified and equalized receive serial data 124 with the phase of the feedback signal, and produces a current signal based on the phase difference.

[0043]   The phase detection module 114 provides the current signal to loop filter 116, which converts it into a control voltage that controls the output frequency of the voltage controlled oscillator 118. At this point, the output of the voltage controlled oscillator 118 corresponds to a recovered clock 138 in steady state operation. The recovered clock 138

is provided to the divider module 122, the data detection circuit 110 and to the serial-to-parallel module 104. The data detection circuit 110 utilizes the recovered clock 138 to produce recovered data 136 from the amplified and equalized receive serial data 124. The divider module 122 divides the recovered clock 138, in accordance with a parallel receive and programmable logic clock setting 134, to produce a parallel receive clock 94 and a programmable logic receive clock 96. Note that the serial receive clock setting 132 and the parallel receive and programmable logic clock setting 134 are part of the programmed deserialization setting 66 provided to the programmable receive PMA module 40 by the control module 35.

[0044]   The serial-to-parallel module 104, which may include an elastic store buffer, receives the recovered data 136 at a serial rate in accordance with the recovered clock 138. Based on a serial-to-parallel setting 135 and the parallel receive clock 94, the serial-to-parallel module 104 outputs the receive parallel data 54. The serial-to-parallel setting 135, which may be part of the programmed deserialization setting 66, indicates the data rate and data width of the receive parallel data 54.

[0045]   Figure 4B illustrates a schematic block diagram of a programmable transmit PMA module 38 that includes a phase locked loop 144, a parallel-to-serial module 140, and a line driver 142. The phase locked loop 144 includes a phase detection module 146, a loop filter 148, a voltage controlled oscillator (VCO) 150, a divider module 154, and a divider module 152.

[0046]   The phase detection module 146 compares the phase and/or frequency of the reference clock 86 with the phase and/or frequency of an output produced by divider module 154. The phase detection module 146 generates a current signal to represent the phase and/or frequency difference between the reference clock 86 and the feedback oscillation. The loop filter 148 converts the current signal into a control voltage

that regulates the output oscillation produced by the VCO 150. Divider module 154, based on a serial transmit clock setting 158, divides the output oscillation of the VCO 150, which corresponds to a serial transmit clock 92, to produce the feedback oscillation. Note that the serial transmit clock setting 158 may be part of the programmed serialization setting 64 provided to the programmable transmit PMA module 38 by the control module 35.

[0047]   Divider module 152 receives the serial transmit clock 92 and, based on a parallel transmit and programmable logic clock setting 160, produces a parallel transmit clock 88 and a transmit programmable logic clock 90. The parallel transmit and programmable logic clock setting 160 may be part of the programmed serialization setting 64.

[0048]   The parallel-to-serial module 140 receives the transmit parallel data 48 and produces therefrom a serial data stream 156. To facilitate the parallel-to-serial conversion, the parallel-to-serial module 140, which may include an elastic store buffer, receives a parallel-to-serial setting to indicate the width of the transmit parallel data 48 and the rate of the transmit parallel data, which corresponds to the parallel transmit clock 88. Based on the parallel-to-serial setting, the serial transmit clock 92 and the parallel transmit clock 88, the parallel-to-serial module 140 produces the serial data stream 156 from the transmit parallel data 48.

[0049]   The line driver 142 increases the power of the signals forming serial data stream 156 to produce the transmit serial data 50. The line driver 142, which is described in greater detail in co-pending patent applications related applications listed above and having the same filing date as the present application, may be programmed to adjust its pre-emphasis settings, slew rate settings, and drive settings via a pre-emphasis control signal 161, a pre-emphasis setting signal 162, a slew rate setting signal 164, an idle state setting 165 and a drive current setting 166.

The pre-emphasis control signal 161, the pre-emphasis setting signal 162, the slew rate setting signal 164, the idle state setting 165 and the drive current setting 166 may be part of the programmed serialization setting 64. As one of average skill in the art will appreciate, while the diagram of Figure 4B is shown as a single-ended system, the entire system may use differential signaling and/or a combination of differential and single-ended signaling.

[0050]   Figure 5 is a schematic block diagram of a ring oscillator according to an embodiment of the present invention. A ring oscillator, as is known to one of average skill in the art, utilizes a plurality of delay stages to provide a loop gain equal to or greater than one and a 180 degree phase shift between an input and an output, thereby sustaining oscillation. As can be seen in Figure 5, a ring oscillator 170 includes a plurality of delay stage circuits, namely, delay stage circuits 174, 178 and 182, to provide the necessary phase shift and delay to sustain oscillation. Frequency control logic 192 operably couples a frequency control signal to each delay stage circuit. As will be described in the following figures, frequency control logic 192 selectively adjusts a resistive load in each delay stage circuit to set a ring oscillator delay value and, therefore, a selected oscillation frequency. Each delay stage circuit also produces a peak amplitude at the selected oscillation frequency thereby providing the gain necessary to sustain oscillation. As can also be seen in Figure 5, a feedback loop is created by coupling an output oscillation signal from delay stage circuit 182 to an input of delay stage circuit 174. The output of delay stage circuit 174 is coupled, in turn, to an input of delay stage circuit 178. An output of delay stage circuit 178 is coupled to an input of delay stage circuit 182 to complete the feedback loop. The output oscillation signal is further coupled to a buffer 190, which presents a high impedance to the ring oscillator and also amplifies the output oscillation signal. An external bias

circuit 186 produces bias signals to the delay stage circuits
to bias them in an active operating region and to provide a
fine control on the delay of each delay stage circuit.

[0051]   Ring oscillators can be used as a voltage
controlled oscillator (VCO) in a phase-locked loop (PLL),
such as PLL 112 of Figure 4A (OR PLL 144 OF FIG. 4B). When
used in a PLL, external bias circuit 186 receives a control
voltage from a loop filter of the PLL. The control voltage
is proportional to the phase difference between a reference
clock and the output of the ring oscillator to the control
voltage in one embodiment of the invention. Generally, the
control voltage magnitude corresponds to a specified
frequency of oscillation. Accordingly, changes in the
control voltage result in corresponding changes in the bias
signals produced to the delay stage circuits therefore
resulting in a corresponding change in the delay provided by
the delay stage circuits. The change in delay time results
in a change of oscillation frequency of the ring oscillator.
The control voltage coupled to external bias circuit 186,
therefore, adjusts the delay of the delay stage circuits to
phase lock the output oscillation signal to the reference
signal.

[0052]   Although three delay stage circuits are shown in
Figure 5, the number of delay stages can be any number as
long as they produce the required loop gain and phase shift
from the input oscillation signal to the output oscillation
signal. In one embodiment of the present invention, six
delay stage circuits are used to produce the required phase
shift and desired oscillation frequency. Generally, the
period of the oscillation frequency is twice the total delay
of the ring oscillator circuit.

[0053]   Figure 6 is a schematic block diagram of an NMOS
delay stage circuit according to one embodiment of the
present invention. A delay stage circuit 194 can be used for
any of delay stage circuits 174-182 of Figure 5. A
differential transistor pair 198 comprises MOSFET transistors

M1 and M2, receives an input oscillation signal and produces
an output oscillation signal that is delayed relative to the
input oscillation signal. The total delay through the ring
oscillator will be the delay through each delay stage circuit
multiplied by the number of delay stage circuits in the ring
oscillator. An active load 202, coupled to each drain of the
differential transistor pair 198, provides level shifting
from input to output and additionally provides a peaking
function at the oscillation frequency. Active load 202
comprises a pair of MOSFET devices (load transistors),
namely, MOSFETs M3 and M4, coupled between differential
transistor pair 198 MOSFET transistor drains and a supply. A
selectable resistive load R_L is coupled between the supply
and the gates of MOSFET devices M3 and M4, respectively. A
capacitance Cgs is shown coupled between the gate and source
of MOSFET devices M3 and M4. As is known to one of average
skill in the art, capacitance Cgs is an internal gate-to-
source capacitance of the MOSFET device. For the purposes of
discussion, however, capacitance Cgs is shown as a separate
element connected to MOSFET devices M3 and M4.

[0054]   Selectable resistive load R_L, when coupled to
internal gate-to-source capacitance of MOSFETs M3 and M4,
produces a desired R-C time constant to set the input-output
delay of the differential transistor pair 198. The R-C time
constant set by the selectable resistive load R_L and the
gate-to-source capacitance of each delay stage defines the
total phase shift and, therefore, the oscillation frequency
of the ring oscillator. Normal manufacturing processes
produce slight variations in device values so the R-C values
form a coarse frequency control and provide for a frequency
of operation. A bias signal produced by external bias
circuit 186 based on a control voltage from an external
circuit (typically from a loop filter in a PLL circuit)
effectively forms a fine frequency control to shift the
oscillation frequency around the oscillation point defined by
R_L and Cgs.

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[0055]   As can be seen in Figure 6, the output oscillation
signal is coupled to one terminal of capacitance Cgs, which
is in turn coupled to a resistor of selectable resistive load
(collectively "R_L"). This forms an effective high pass
filter which further causes a peak response at a frequency of
oscillation determined by R_L and Cgs. To change the
frequency of oscillation, selectable resistive load R_L is
adjusted, in one embodiment of the invention, from
approximately 75 Ohms to over 3,000 Ohms thereby defining a
range of oscillation frequencies from 2.5 GHz to 5 GHz.

[0056]   Figure 7 is a schematic block diagram of the NMOS
delay stage circuit of Figure 6 illustrating the adjustment
of selectable resistive load R_L to set an oscillation
frequency. As can be seen in Figure 7, selectable resistive
load 204 has been replaced with a plurality of parallel
coupled resistors, namely, resistors R1, R2, R3 and R4.
Resistors R2, R3 and R4 may be formed as resistor configured
MOSFETs or as traditional resistive elements. Resistors R2,
R3 and R4 are switched into the delay stage circuit by
selectable switches S1, S2 and S3 by frequency control logic
192. Selectable switches S1, S2, and S3 are MOSFET devices
controlled by logic signals from frequency control logic 192
in the described embodiment, though other switching devices
may readily be used. When biased into the triode region, the
selectable switches (MOSFET devices) have a very low
resistance, and when biased to an off condition have a very
high resistance thereby effectively connecting the parallel
coupled resistors into and out of the delay stage circuit.

[0057]   Parallel coupled resistors R1 through R4 are
further scaled for desired operating frequencies when
selectively coupled to capacitance Cgs. Resistors R1 are
permanently connected while resistors R2, R3 and R4 are
selectively coupled in parallel to resistors R1 to
selectively adjust a total resistive value (to reduce total
resistance in the configuration as shown). Frequency control
logic 192 selects resistors R2, R3, and R4 in pairs to set

the R-C time constant of the delay stage. For example, when frequency control logic 192 closes a switch to select resistors R2, it closes the S1 switch connected to MOSFET devices M3 and M4.   When frequency control logic 192 selects one of the parallel coupled resistors thereby setting a coarse operating frequency, external bias circuit 186 provides a fine frequency adjustment by adjusting the operating current through MOSFET devices M1 and M2 of differential transistor pair 198. The operation of frequency control logic 192 may be one of manual operation or automatic operation as is known to one of average skill in the art.

[0058]   Figure 8 is a schematic block diagram illustrating gate-to-source capacitance in an N-channel MOSFET. A capacitor is formed when two parallel plate conductors separated by an insulator are charged with a voltage potential. The capacitance is directly proportional to the area of the parallel plates and inversely proportional to the distance separating the parallel plates. As shown generally at 206, the NMOS channel MOSFET is formed by depositing two heavily doped n-type (n+) regions on a p-type substrate. An insulating oxide layer is deposited on the p-type substrate connecting the two n+ regions. A conducting material is deposited on the oxide layer to create the gate. The source and drain are created by depositing a conductive material over the two n+ regions.

[0059]   When a positive voltage is applied to the gate, a conductive channel is formed in the p-type substrate beneath the oxide layer thereby creating a conduction channel between the drain and source. As can be seen in detail A, this creates a pair of parallel conductors (gate and channel) separated by an insulator (dielectric) (oxide layer), i.e., a capacitor. The capacitance of the gate-to-source capacitor is directly proportional to the width and length of the channel and inversely proportional to the oxide layer thickness. In one embodiment of the invention, the width of the channel is formed to be 100 microns, while the length of the channel is

formed to be 0.3 microns so as to yield a more predictable capacitive value than is provided by the minimum capacitive value of typical IC processes.

[0060]   When MOSFET 206 is biased in the triode region, the channel is substantially of uniform depth from drain-to-source thus forming a gate-to-source capacitance and a gate-to-drain capacitance. The MOSFET of an embodiment of the present invention is biased in the saturation region. As is known to one of average skill in the art, the saturation region channel is tapered from drain to source with the drain end of the channel substantially pinched off. Therefore, the capacitance formed by the gate and channel is almost entirely due to the gate-to-source capacitance.

[0061]   Figure 9 is a graph of an NMOS delay stage frequency response according to one embodiment of the present invention. As can be seen in Figure 9, a plurality of frequency response peaks represents the coarse frequency control as selected by frequency control logic 192 of Figure 7. The feed forward affect of capacitance Cgs and the resulting high pass filter formed by Cgs and the parallel coupled resistors produces the peak response at the oscillation frequency. The cell can be configured so the low frequency gain is less than one while providing gain greater than one at the oscillation frequency. The oscillation frequency may also be increased or decreased based on changes in the bias signal produced by external bias circuit (external bias circuit 186 of Figure 5). Also illustrated in Figure 9 is a frequency response curve of the NMOS delay stage circuit without the feed forward signal from capacitance Cgs. The gain of this response curve rolls off at higher frequencies rendering the circuit unable to sustain oscillations.

[0062]   In one embodiment of the invention, the parallel coupled resistors are selected, in conjunction with typical values of the gate-to-source capacitance, to produce oscillation frequencies of 2.5, 3.125, 4.0 and 5.0 GHz. As

can be further seen, without the feed forward signal due to Cgs, the output oscillation signal would roll off at higher frequencies. With the feed forward signal, however, the output amplitude peaks as a function of frequency with a gain of approximately 4 times that of the peak without the feed forward signal. This peaking has several benefits including its usefulness in noise reduction.

[0063]   Figure 10 is a schematic block diagram of an alternate embodiment of the present invention. Referring now to Figure 10, a PMOS delay stage circuit comprises a differential transistor pair 208, comprising MOSFET transistor M5 and M6, coupled to receive an input oscillation signal and to produce therefrom an output oscillation signal characterized by a delay relative to the input oscillation signal. An active load 210 is further coupled to the drains of differential transistor pair 208. Active load 210 comprises current mirrors and selectable loads 212 and 212′ coupled to each of the drains of differential transistor pair 208 that defines the delay of the delay stage circuit and, therefore, the oscillation frequency of the ring oscillator. An external bias circuit 214 further provides a bias signal to produce a fine adjustment on the oscillation frequency.

[0064]   A current mirror comprising MOSFET device M7, current mirror reference device M9, and a current source 216 is coupled in parallel with selectable load 212 comprising adjustable capacitive device C1 and adjustable resistive device R5. Current mirror reference device M9 and current source 216 produce a reference current that is reproduced by MOSFET device M7 as is known by one of average skill in the art. Similarly, a current mirror reference device M10 and a current source 218 produce the reference current that is mirrored by MOSFET device M8. Current sources 216 and 218 determine the reference current through diode connected current mirror reference devices M9 and M10 thereby setting a constant source-to-gate voltage. The source-to-gate voltage is coupled to the gates of MOSFET devices M7 and M8 to

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produce a current in the MOSFET devices. The current produced in MOSFET devices M7 and M8 will be proportional to the current in the current mirror reference devices, the proportionality determined by the respective sizes (scaling) of MOSFET device M7 relative to current mirror reference device M9 and MOSFET device M8 relative to current mirror reference device M10 if the devices are biased in the saturation region. In one embodiment, however, the load devices are biased in the linear region. Accordingly, the proportionality in the scaling would not necessarily be reflected in the relative current flows since current flow is a function of bias signal levels. Current source 216 also allows adjustment of a feedback point common mode.

[0065]   Adjustable capacitive devices C1 and C1' and adjustable resistive devices R5 and R5' of selectable loads 212 and 212' are connected from gate-to-source and from gate-to-drain, respectively, on each of the pair of MOSFET devices M7 and M8. The delay value of the PMOS delay stage is determined by the R-C values of adjustable resistive device R5 (and R5') and adjustable capacitive device C1 (and C1').

[0066]   Figure 11 is a schematic block diagram of a PMOS delay stage circuit according an alternate embodiment of the present invention. Figure 11 illustrates the adjustable resistive device and adjustable capacitive device of Figure 10 as comprising capacitive devices C1 through C4 (and C1' through C4') and resistive devices R5 through R8 (and R5' through R8'). As can be seen in Figure 11, resistive devices R5 and R5' and capacitive devices C1 and C1' are permanently coupled across each of the pair of MOSFET devices M7 and M8, respectively. Additional, the source-to-gate capacitance (not shown) of MOSFETs M7 and M8 is coupled in parallel with capacitive devices C1 through C4 and C1' through C4', respectively.

[0067]   The scaled parallel coupled resistive devices R5 through R8 and R5' through R8'', and scaled parallel coupled capacitive devices C1 through C4 and C1' through C4' are

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selectively coupled into the PMOS delay stage by switch logic
220. In operation, switch logic 220 selects one or more
resistive and capacitive devices to select a delay of the
delay stage and consequently the operating frequency of the
ring oscillator. Switch logic 220 selects a capacitive
device each time it selects a resistive device for each of
the pair of MOSFET devices M7 and M8 and vice-versa. For
example, when switch logic 220 closes, switches S4/S4',
capacitive elements C4/C4' and resistive elements R8/R8' are
selectively coupled to the gate terminals of MOSFET devices
M7 and M8. Similarly, switch logic 220 can selectively close
switches S5/S5' and S6/S6' as necessary to produce a desired
delay which further characterizes the oscillation frequency
of the ring oscillator. In an alternate embodiment, the
capacitors may be selected independently from the resistors
and vice-versa. As is known to one of average skill in the
art, switches S4 through S6 (and S4' through S6') are
typically formed as MOSFET switches characterized by a very
low on resistance and a very high off resistance. At least
one resistive device may be formed as a resistor configured
MOSFET or a traditional resistive device. Similarly, at
least one capacitive device may be formed as a capacitor
configured MOSFET or a traditional capacitive device.

[0068]   Figure 12 is a graph of a PMOS delay stage response
according to one embodiment of the present invention. The
PMOS delay stage utilizes negative feedback from the output
oscillation signal back to MOSFET devices M7 and M8. At low
frequencies, the negative feedback is coupled through the
resistive elements, namely, resistive elements R5 through R8
(and R5' through R8') of Figure 11, to the gates of MOSFET M7
and M8 and reduces gain as shown by response line 222 away
from the oscillation frequency. At the oscillation
frequency, the R-C value of selectable load 212 is at a
maximum value as illustrated by response line 224. As the
frequency increases beyond the peak value, the decreasing
impedance value of the capacitive elements of selectable load

212 reduces the gain of MOSFET devices M7 and M8 causing the peak response to roll off. In one embodiment of the present invention, capacitive devices C1 through C4 (and C1' through C4') and resistive devices R5 through R8 (and R5' through R8') are selected to define a total delay through the ring oscillator resulting in oscillation frequencies of 2.5, 3.125, 4.0 and 5.0 GHz.

[0069]   Figure 13 is a flowchart of a method according to one embodiment of the present invention. A delay stage circuit receives a frequency control signal (step 228) that selects a delay of the delay stage circuit and ultimately an oscillation frequency of a ring oscillator. The invention further includes selectively coupling at least one resistor to an active load (step 232) and optionally coupling at least one capacitor to the active load (step 236). The at least one resistor and the at least one capacitor generate an R-C time constant of the active load that determines the delay of the delay stage circuit. The delay stage receives a bias signal to adjust a frequency of oscillation (step 240). The bias signal determines an operating current level in a differential transistor pair further adjusting the delay of the delay stage circuit. The differential transistor pair receives an input oscillation signal (step 244). The delay produced by the bias current and by the active load R-C time constant will produce a corresponding delayed output oscillation (step 248).

[0070]   The invention disclosed herein is susceptible to various modifications and alternative forms. Specific embodiments therefore have been shown by way of example in the drawings and detailed description. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the claims.